degradation associated with hot carrier stress, and said concentration of deuterium increasing the resilience of the field effect transistor to channel hot carrier stress.

77. (New) A semiconductor device according to claim 76 wherein the semiconductive layer comprises silicon, and the gate dielectric film includes a silicon compound.

78. (New)) A semiconductor device according to claim 77 wherein said silicon compound comprises a an oxygen or a nitrogen containing silicon compound.

REMARKS:

A. Applicant requests that an interference be declared between this application and Patent 6023093 issued February 8, 2000 to Richard W. Gregor and Isik C. Kizilyalli, based on Application Serial No. 847704 filed April 28, 1997. Claims 66-78 added by this amendment are presented within one year of the issue date of Patent 6023093.

B. The present application 09/160,657 was filed on September 25, 1998 as a continuation of Application No. 09/020,565 filed January 16, 1998, which is a continuation of International Application PCT/US97/00629 filed January 16, 1997 which designated the United States, which is a continuation-in-part of Application No. 08/587,411 filed January 16,1996, now issued as US patent 5,872,387. As shown below, claims 66-78 are supported by the disclosure of Application No. 08/587,411 filed January 16, 1996 from which the present application derives priority under 37 CFR 1.120 and the effective filing date of claims 66-78 is January 16, 1996.

C. The following is proposed as a count in the requested interference:

Proposed Count: An improved semiconductor transistor device having a transistor gate and a film located adjacent said transistor gate and having a concentration of deuterium within said film, wherein the improvement comprises:

a concentration of at least about 10^{16} cm^{-3} of said deuterium being present in said film, said transistor device susceptible to degradation associated with hot carrier stress, said concentration of deuterium substantially reducing said degradation associated with said hot carrier stress.

D. Claim 1 in Patent 6023093 corresponds to the proposed count.

E. New claims 66-74 correspond to claims 1-9 of Patent 6023093 except that errors in the dependencies of claims 3 and 6 of the patent have been corrected in claims 68 and 71 and claim 71 recites only "a complementary metal oxide semiconductor" and omits reference to a "silicon submicron" because of lack of antecedent basis.

New claims 66 -78 are supported by the disclosure of the present application ('657 application) and by Application No. 08/587,411 ('411 application) at least by the following passages:

Claim	'657 application: (Also application PCT/US97/00629)	'411 application
Claim 66:	Page 8, line 14 to page 9, line 13; page 9, line 15 to page 13, line 11; page 18, line 10 to page 22, line 12, noting, e.g. page 21 lines 20-27. page 22, line 14 to page 23, line 3. Lyding Affidavit (see discussion below).	Page 7, line 13 to page 8, line 10; page 8, line 12 to page 11, line 25; page 8, line 12 to page 11, line 25; page 14, line 1 to page 17, line 21, noting, e.g. page 17, lines 2-10; page 17, line 2 to page 18, line 10. Lyding Affidavit (see discussion below).
Claim 67:	Page 10, lines 20 -27 and page 11, lines 7-9.	Page 9, lines 15-20 and page 10, lines 1-3.
Claim 68:	Page 10, lines 20-27 and page 11, line 24 to page 12, line 4.	Page 9, lines 15-20 and page 10, lines 17-23.

Claim 69:	Page 10, line 27 to page 11, line 9.	Page 9, line 20 to page 10, line 3.
Claim 70:	Page 10, lines 20-27.	Page 9, lines 15-20
Claim 71:	Page 9, line 15 to page 10, line 6.	Page 8, line 12 to page 9, line 2.
Claim 72:	Page 10, lines 8-16.	Page 9, lines 4-11.
Claim 73:	Page 10, lines 8-16.	Page 9, lines 4-11.
Claim 74:	Page 10, line 8 to page 11, line 9 and page 11, line 24 to page 12, line 4.	Page 9, line 8 to page 10, line 3 and page 10, lines 17-23.
Claim 75:	Page 8, line 14 to page 9, line 13; page 9, line 15 to page 13, line 11; page 18, line 10 to page 22, line 12, noting, e.g. page 21 lines 20-27. page 22, line 14 to page 23, line 3, Lyding Affidavit (see discussion below).	Page 7, line 13 to page 8, line 10; page 8, line 12 to page 11, line 25; page 14, line 1 to page 17, line 21, noting, e.g. page 17, lines 2-10; page 17, line 2 to page 18, line 10. Lyding Affidavit (see discussion below).
Claim 76	Same as claim 75.	Same as claim 75.
Claim 77:	Page 11, line 16 to page 12, line 4.	Page 10, lines 9-23.
Claim 78:	Page 10, lines 20-27.	Page 9, lines 14-20.

F. As shown in Section E. above, the disclosures of application 09/160,657 and application 08/856,411 (as well as of the intervening applications in the priority chain under 37 CFR 120) satisfy the requirements of 35 US 112, first paragraph, by providing adequate written description of the subject matter of the proposed count and of each of new claims 66-78. The feature of the proposed count and new claim 66 that the concentration of deuterium resulting from the disclosed annealing process is "at least about 10^{16} cm^{-3}" is a result of the particular annealing process described in those applications and thus is inherently disclosed by each of those applications, satisfying the criteria contained in MPEP 2163.07(a). This is further demonstrated because the effect of the deuterium content as recited in the count ("said concentration of deuterium

substantially reducing said degradation associated with said hot carrier stress) is the same as explicitly disclosed in both of these applications, (e.g. '657 application at page 22, lines 18-21- "As can be seen, wafers sintered in a deuterium ambient exhibit dramatically higher levels of resilience to channel hot carrier stress"). Regarding new claims 75 and 76, the concentration of deuterium resulting from the recited process steps will be "at least about 10^{16} cm^{-3}" so that these claims are inherently disclosed by application 09/160,657 and its predecessor applications in the priority chain under 37 CFR 120.

For example, Application 09/160,657 includes disclosure at page 18, line 10 to page 22, line 12 of annealing wafers containing NMOS transistor structures (i.e transistors which have a transistor gate and a film - e.g. gate oxide - located adjacent the transistor gate) in which " wafer samples were annealed in an ambient of 10% deuterium in nitrogen for a period of about 1 hour. The temperature was maintained at about 400°C" – see page 21, lines 20-27 of application 09/160,657. As established by the accompanying Lyding Affidavit (see paragraphs 5, 6 and 7) carrying out the annealing process using these parameters produces a semiconductor transistor device having the structural characteristics set forth in the proposed count and claim 66, including a concentration of deuterium of "at least about 10^{16} cm^{-3}", and the device recited in claims 75 and 76 also will include that concentration of deuterium. That these deuterium annealing process parameters result in the stated deuterium concentration level is evidenced by J. W. Lyding, K. Hess and I. C. Kizilyalli, "Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing, *Applied Physics Letters,* **68** (18), pp. 2526-2528, 29 April 1996, (Exhibit A to the Lyding Affidavit – see Lyding Affidavit, paragraph 5). (It is noted that the coauthor Kizilyalli is named as coapplicant in the 6023093 patent.) These results from deuterium annealing of MOS transistor devices under the same ambient, temperature and time conditions as disclosed in the present application, are substantiated by Thomas G. Ference, Jay S. Burnham, William F. Clark, Terence B. Hook, Steven W. Mittl, Kimbal M. Watson, and

Liang-Kai Kevin Han "The Combined Effects of Deuterium Anneals and Deuterated Barrier-Nitride Processing on Hot-Electron Degradation in MOSFET's", *IEEE Transactions on Electron Devices*, vol. 46, No. 4, pp. 747-753, April 1999, (Exhibit C to the Lyding Affidavit – see Lyding Affidavit paragraph 6). The Lyding Affidavit confirms (paragraph 7) that the deuterium annealing process disclosed in Application 09/160,657 would result in a concentration of 75 and 76 at the gate oxide (dielectric film)/silicon (substrate) interface and in the gate oxide of the transistor device disclosed in that application as specified in claim 1 of Patent 6023093 which corresponds to the proposed count and to claim 66 in this application. For similar reasons, that concentration of deuterium also will be present in a device as recited in each of claims 75 and 76.

That Applicants' disclosed annealing process parameters, including those described at page 21, lines 20-27 of application 09/160,657, achieve reduction in degradation associated with hot carrier stress as recited in the proposed count, and in each of claims 66, 75 and 76, is disclosed in application 09/160,657, for example at page 22, line 14 to page 23, line 3 (". . . wafers sintered in a deuterium ambient exhibit dramatically higher levels of resilience to hot channel carrier stress" - page 22, lines 18-21). This effect is confirmed in paragraph 7 of the Lyding Affidavit and is also described in the Lyding, Hess and Kizilyalli publication (Exhibit A to the Lyding affidavit) and substantiated by the Ference, et al. publication (Exhibit C to the Lyding Affidavit).

In summary, the proposed count and each of claims 66-78 is supported by the disclosure of Application 09/160,657 and by the disclosure of Application 08/856,411 from which Application 09/160,657 derives priority under 37 CFR 120, either by explicit disclosure as discussed above or by inherent disclosure because carrying out the annealing process disclosed in the '657 and '411 applications will result in the features of the transistor device as specified in the proposed count and new claim 66, and the concentration of deuterium as recited in each claims 75 and 76 will inherently

be "at least about 10^{16} cm^{-3}." Consequently, Application 09/160,657 (and its predecessor applications in the priority chain under 37 CFR 120) satisfy the requirements of 35 US 112, first paragraph, by providing adequate written description explicitly or inherently (consistent with MPEP 2163.07(a)) of the subject matter of the proposed count and of each of claims 66-78. These conclusions are verified by the Lyding Affidavit, the Lyding, Hess and Kizilyalli publication (Exhibit A to the Lyding affidavit) and substantiated by the Ference, et al. publication (Exhibit C to the Lyding Affidavit).

Entry of claims 66-78 and grant of the request for interference with Patent 6023093 contained herein are solicited.

Date: February 8, 2001
SHARP, COMFORT & MERRETT
13355 Noel Rd. Suite 1340
Dallas, Texas 75240-6838
Tel: (972) 490-3695
Fax: (972) 490-3863

Respectfully submitted,

N. Rhys Merrett
Registration No. 27250